

FIG. 1A

Prior Art

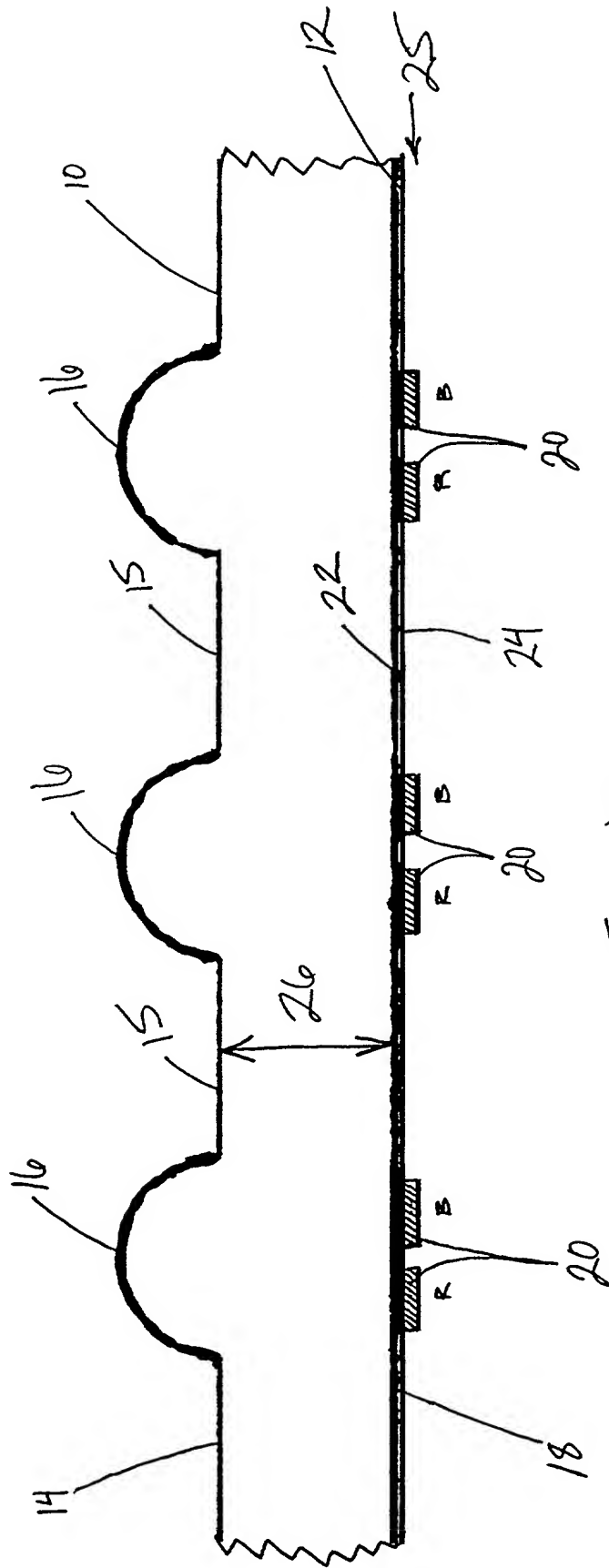


FIG. 1B  
PRIOR ART

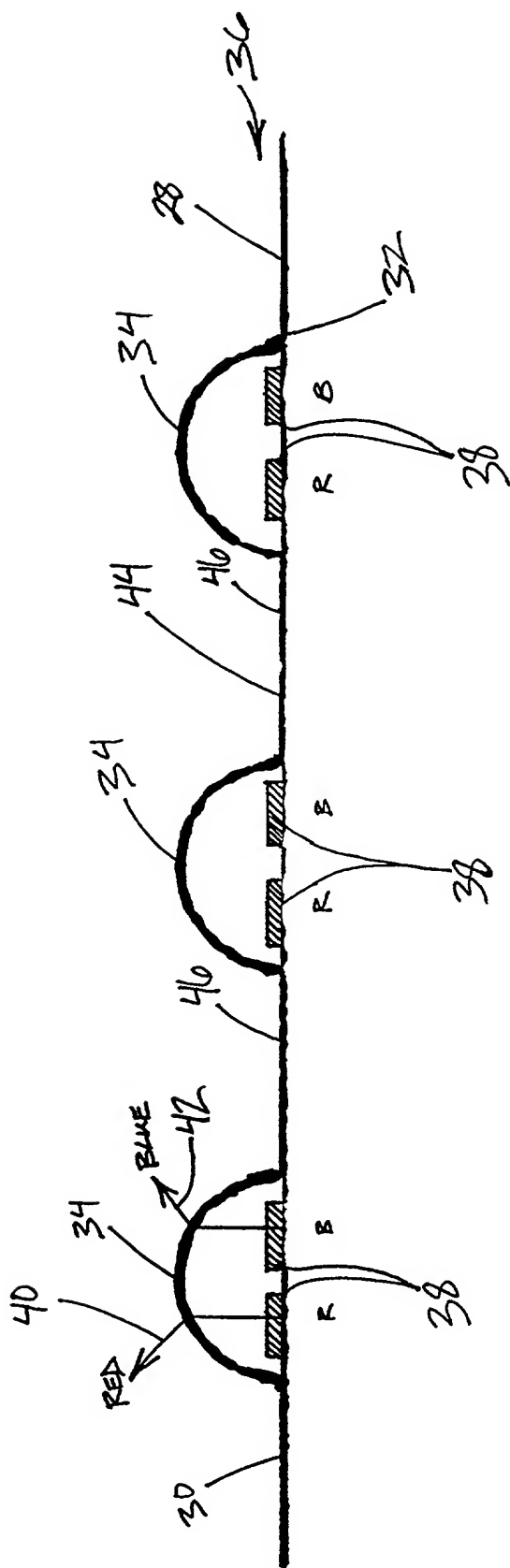


FIG. 2A

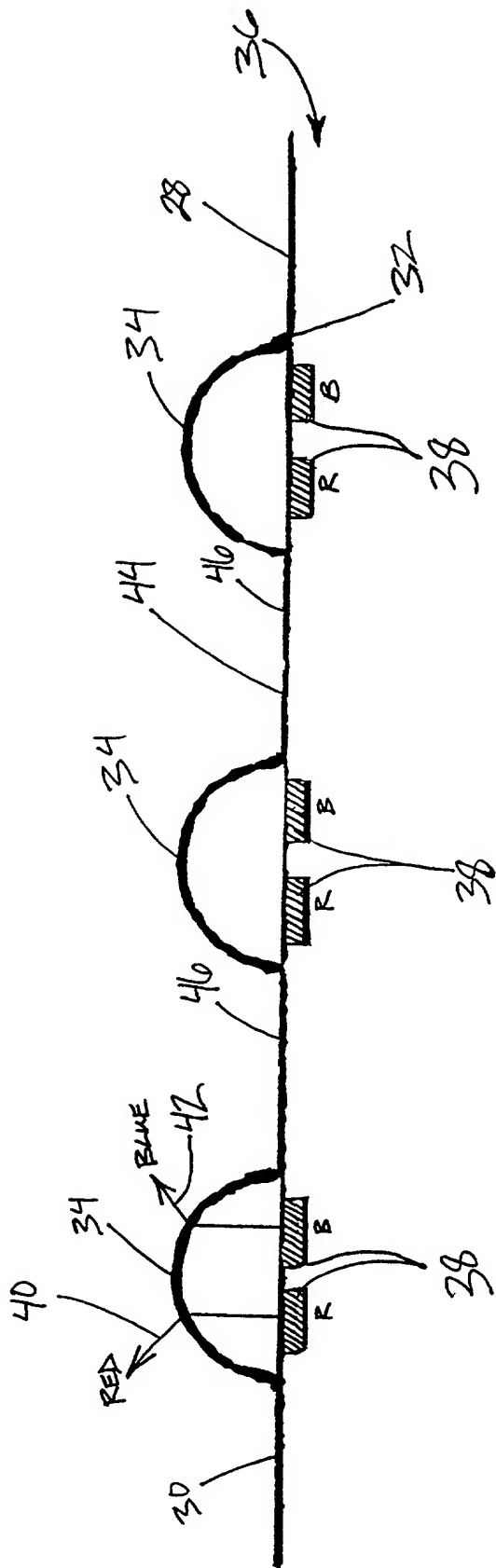


FIG. 2B

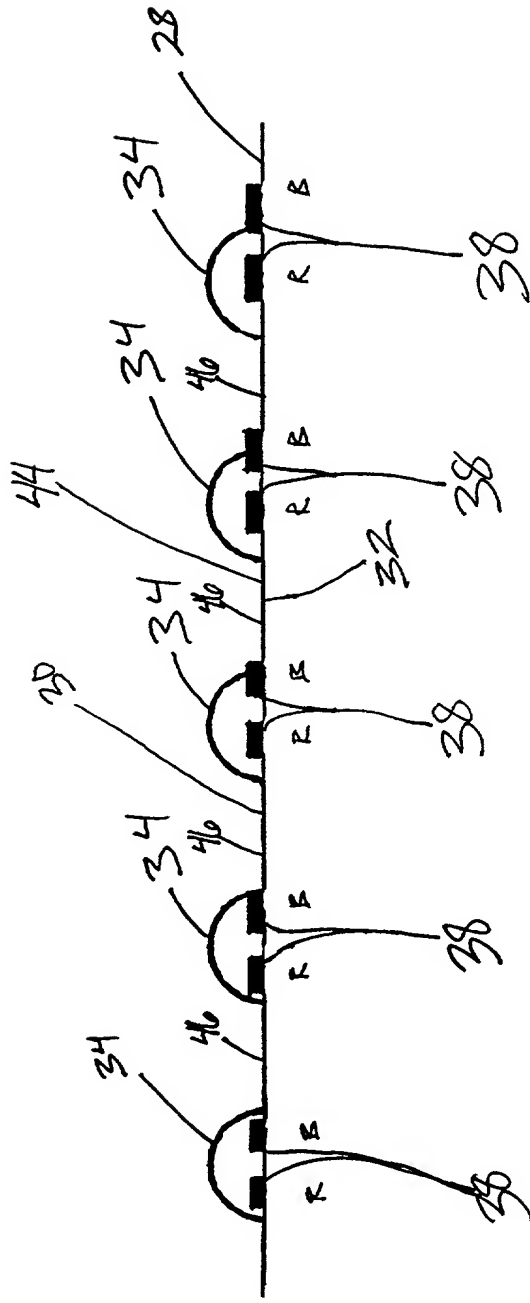


FIG. 3A

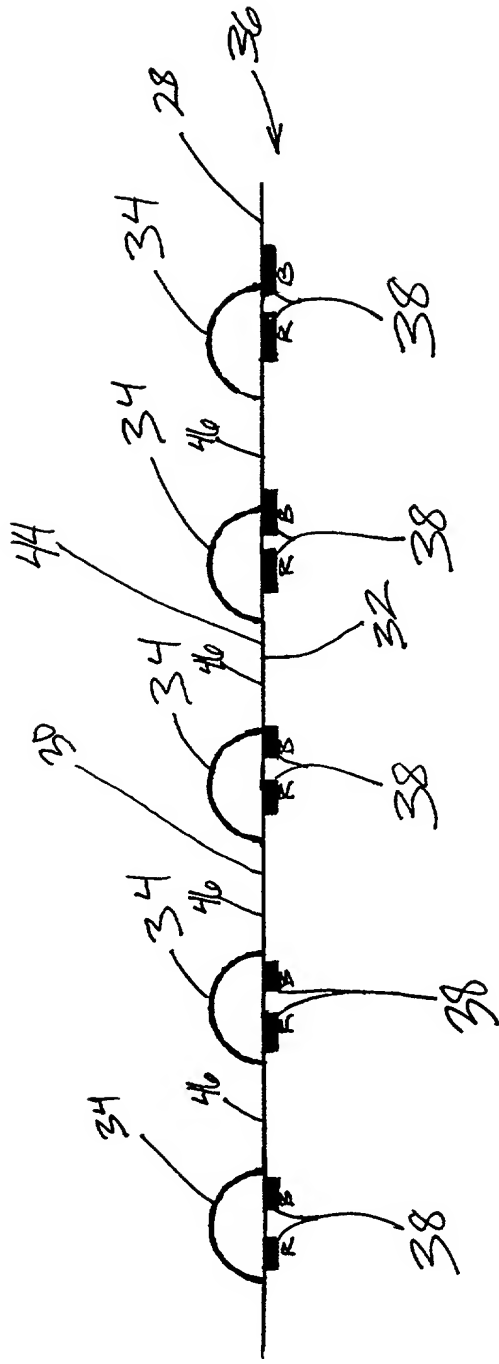


FIG. 3B

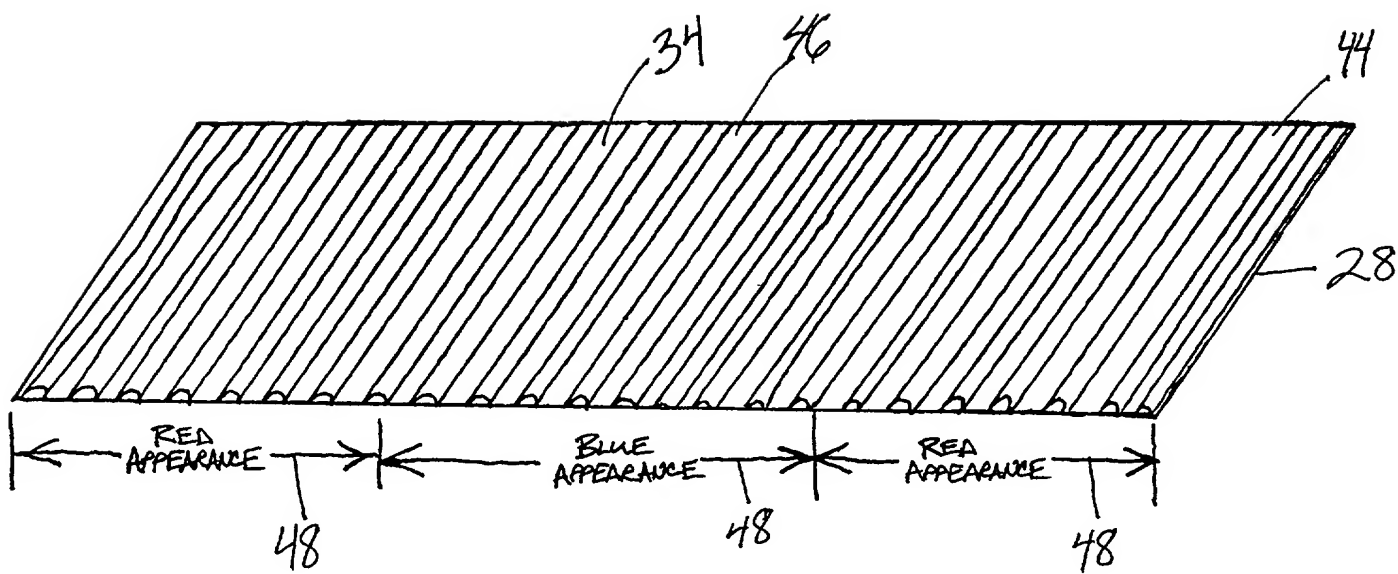


FIG. 4

FIG. 5 is a schematic diagram of a system 50 for processing a signal. The system 50 includes a first processing unit 54, a second processing unit 56, and a third processing unit 56. Each processing unit 54, 56, 56 includes a plurality of input/output ports 60. The first processing unit 54 is connected to the second processing unit 56 via a first connection 62. The second processing unit 56 is connected to the third processing unit 56 via a second connection 62. The first connection 62 is a bidirectional connection, and the second connection 62 is a unidirectional connection. The system 50 is configured to process a signal 58. The signal 58 is input to the first processing unit 54 via a first input port 60. The signal 58 is output from the first processing unit 54 via a first output port 60. The signal 58 is input to the second processing unit 56 via a second input port 60. The signal 58 is output from the second processing unit 56 via a second output port 60. The signal 58 is input to the third processing unit 56 via a third input port 60. The signal 58 is output from the third processing unit 56 via a third output port 60. The system 50 is configured to process a signal 58. The signal 58 is input to the first processing unit 54 via a first input port 60. The signal 58 is output from the first processing unit 54 via a first output port 60. The signal 58 is input to the second processing unit 56 via a second input port 60. The signal 58 is output from the second processing unit 56 via a second output port 60. The signal 58 is input to the third processing unit 56 via a third input port 60. The signal 58 is output from the third processing unit 56 via a third output port 60.

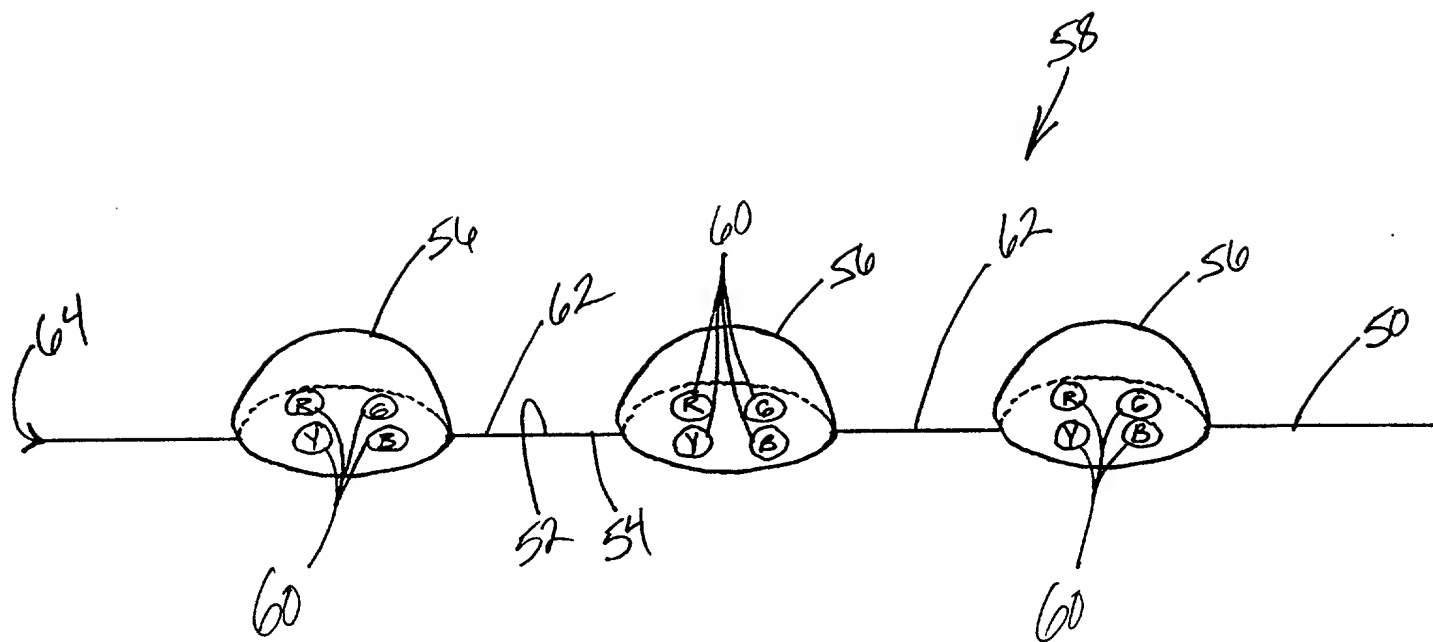


FIG. 5



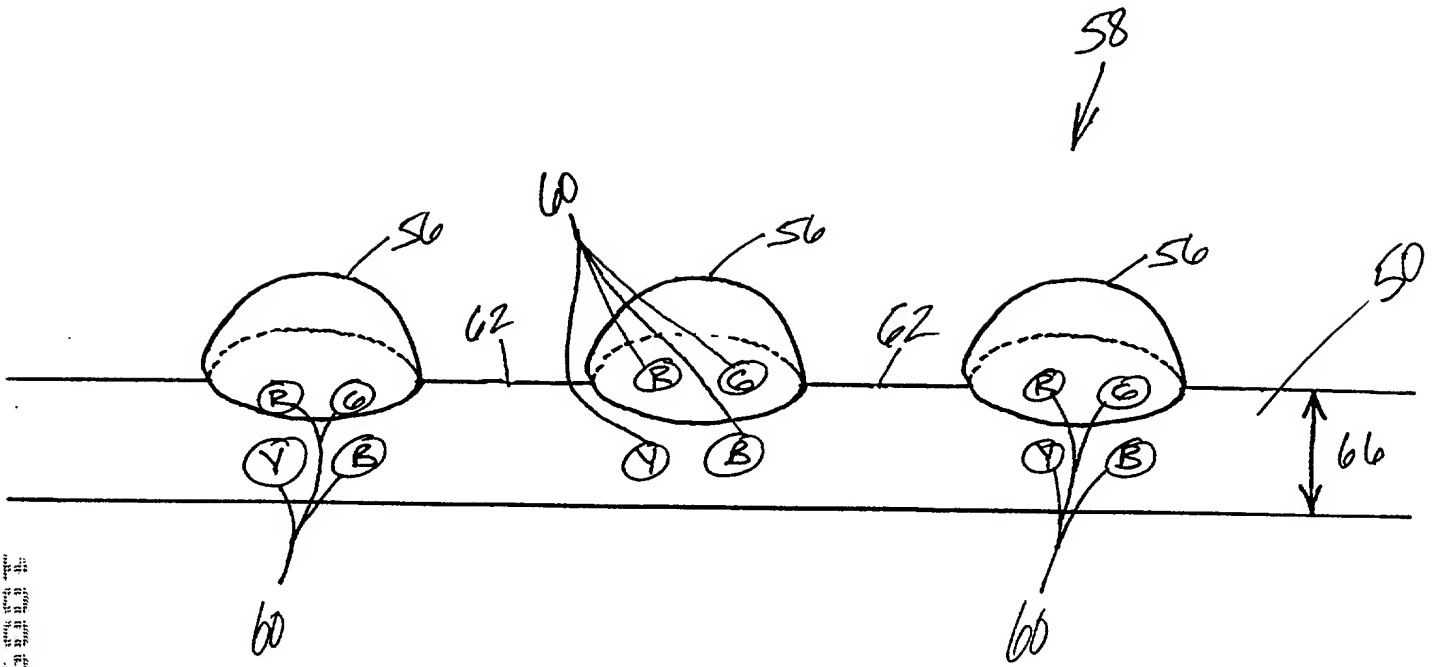


FIG. 6

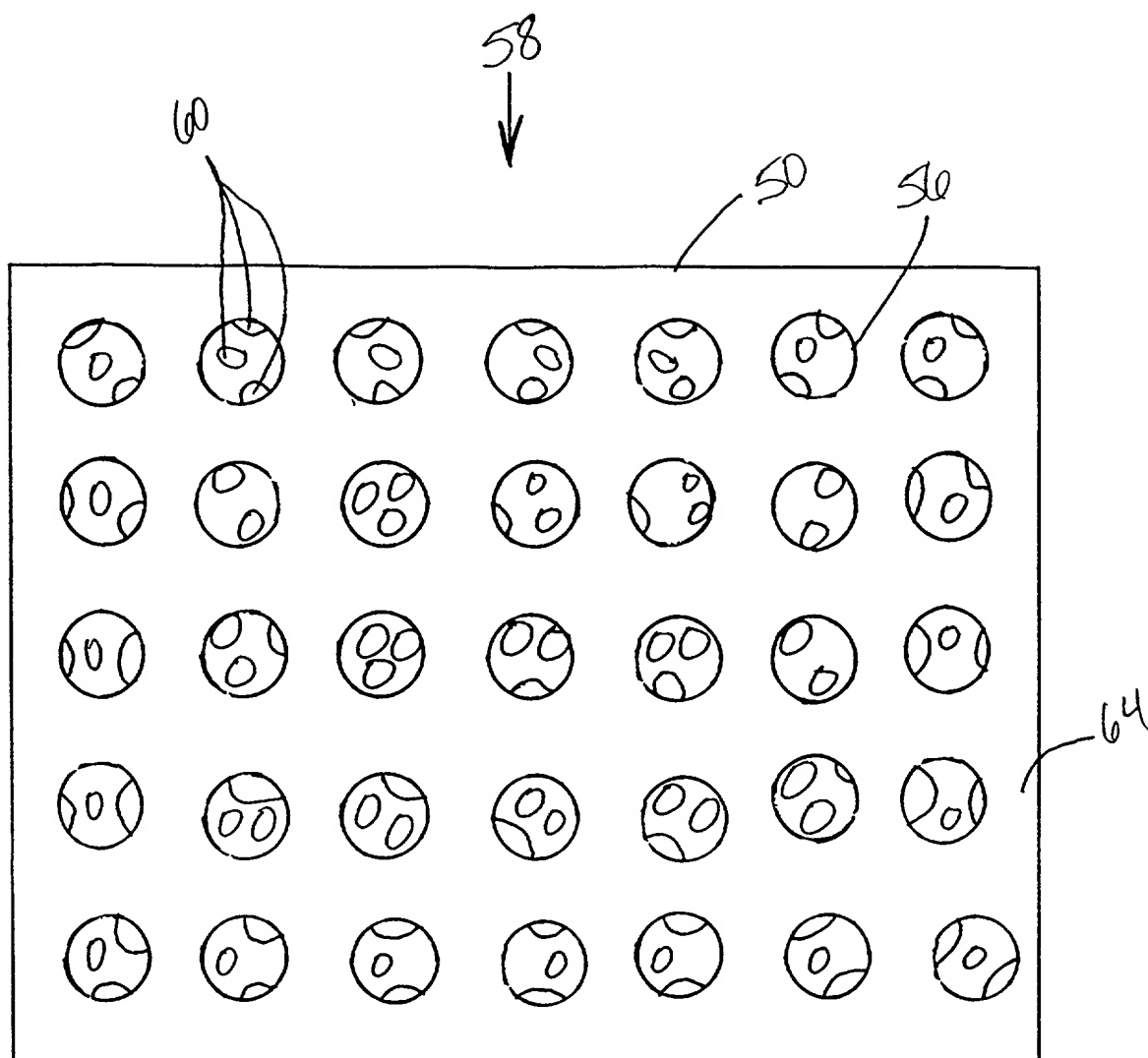


FIG. 7